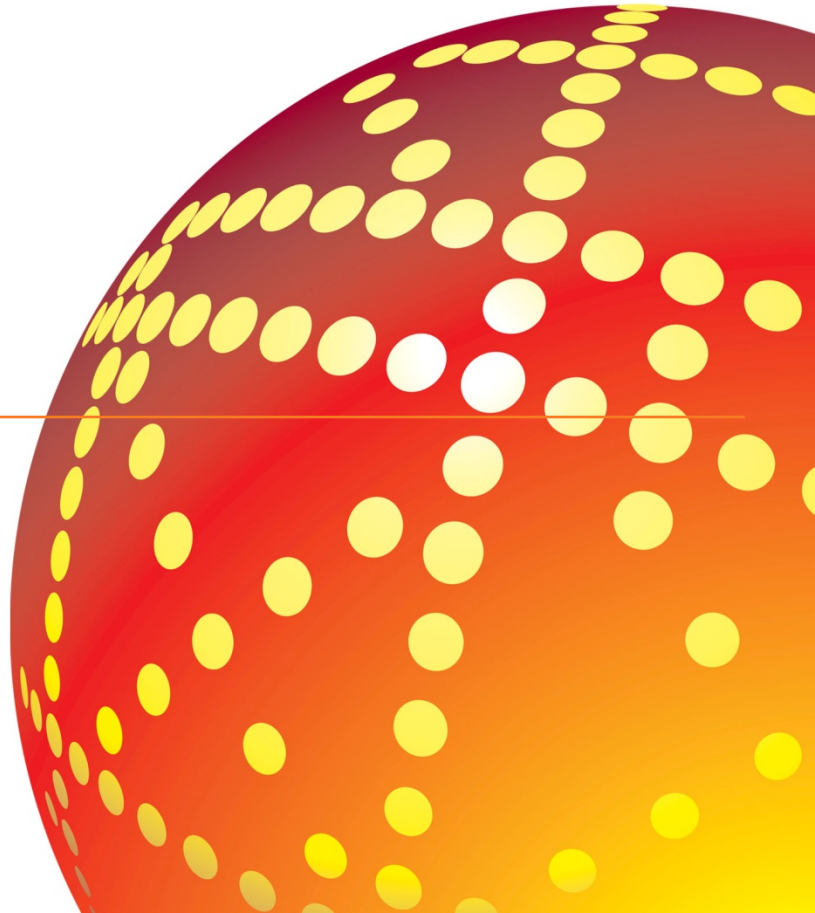
EUV Lithography: Approaching Pilot Production

GLOBALFOUNDRIES



Obert R Wood II

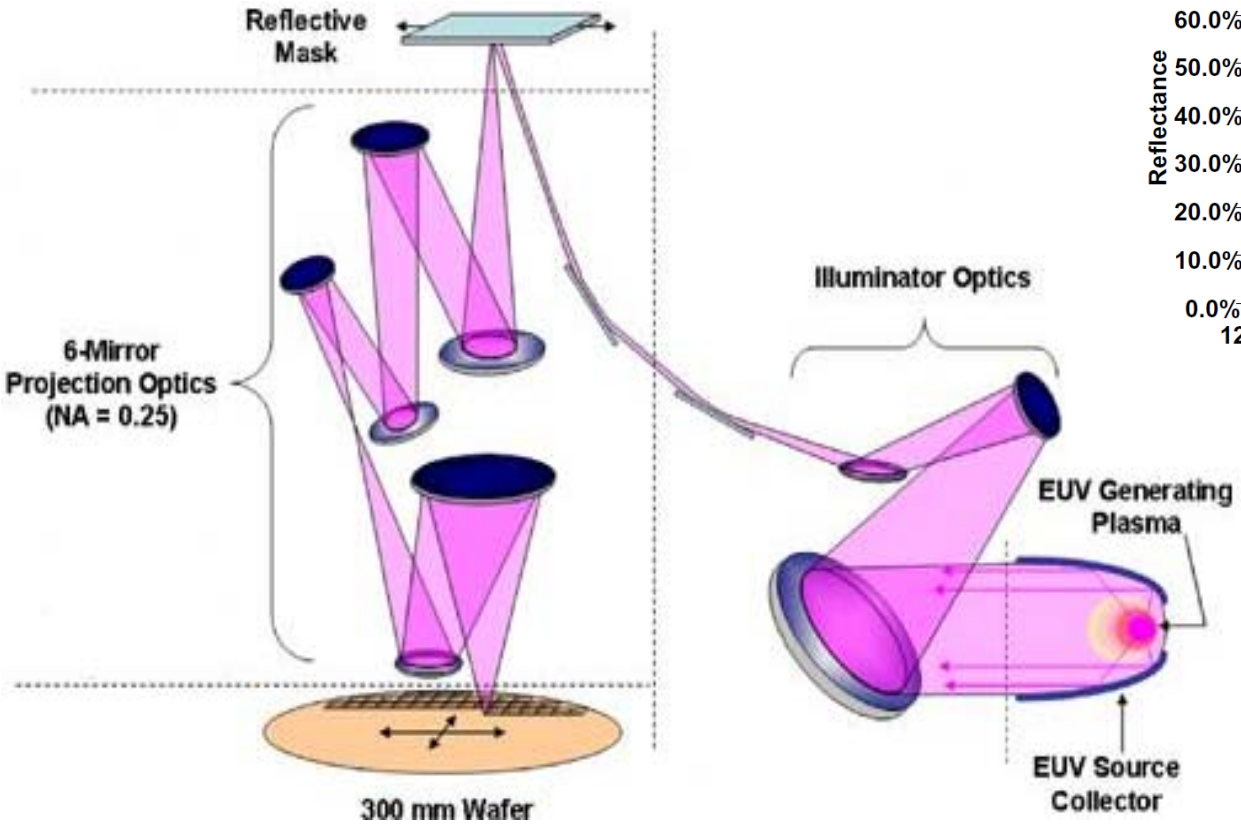
2010 EUV Lithography Workshop
Maui, Hawaii
June 23, 2010

Outline of Presentation

- Introduction
- EUV Device Integration Exercises
  - 45-nm, 22-nm & 16-nm Nodes
- EUV Exposure Tool Status
- EUV Infrastructure Status
  - Masks
  - Sources
  - Resists
- Suggestions for Future Work
- Summary

Extreme Ultraviolet (EUV) Lithography

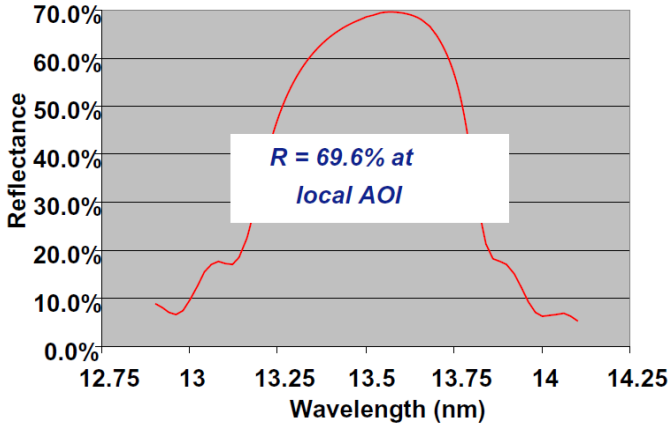
EUV R&D Exposure Tool



Ref: S. Wurm (SEMATECH)

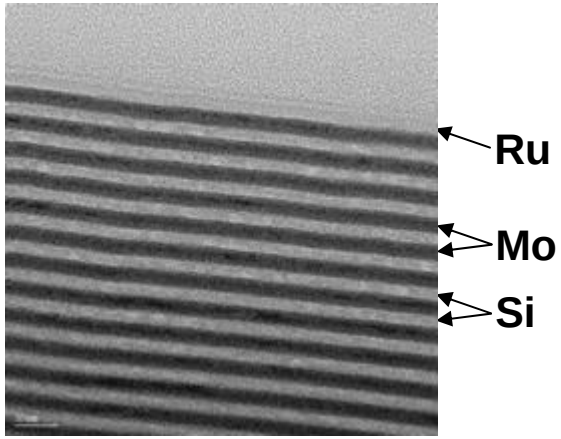
$$HP = k_1 \lambda / NA$$

50 bilayer Mo/Si-based Multilayer



Ref: S. Bruijn (FOM), 2009 EUVL Symp.

Cross section TEM view



Ref: S. Baji (LLNL), Private Communication

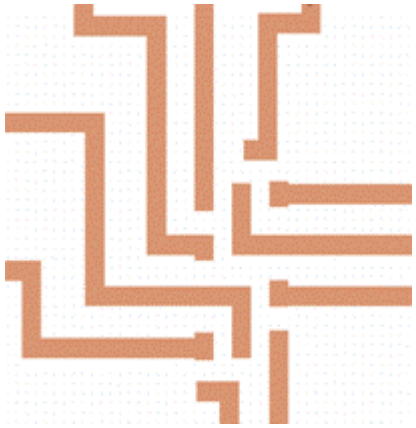
EUV Lithographic Printing

EUVL Advantages

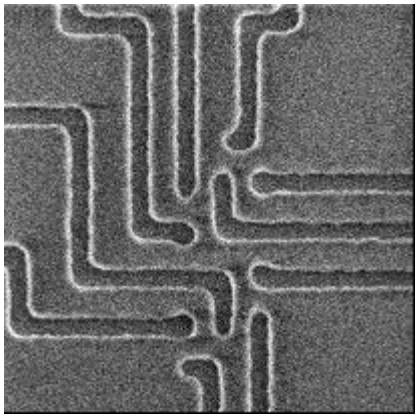
- Return to high k_1 imaging
- Conventional OPC
- Single exposures
- No forbidden pitches
- Relaxation of restricted design rules

$$HP = k_1 \lambda / NA$$

40 nm HP Pattern

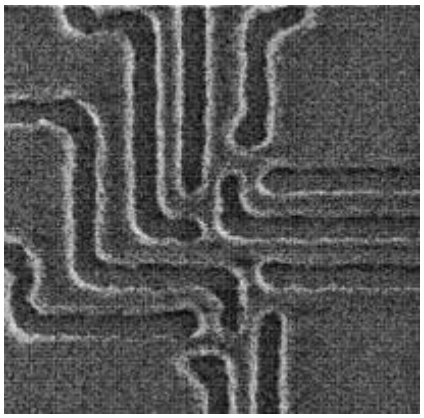


Single Exposure EUV



k_1 = 0.74 (0.25NA)

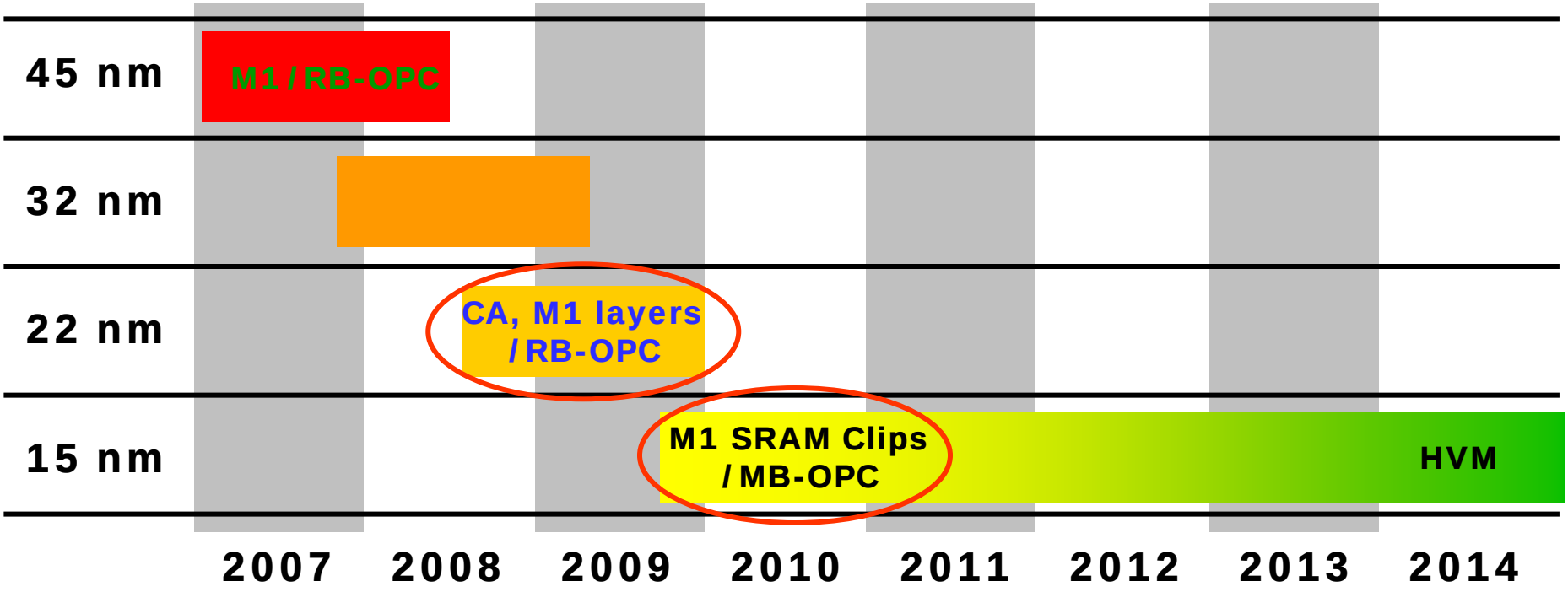
Double Dipole 193i



k_1 = 0.28 (1.35NA)

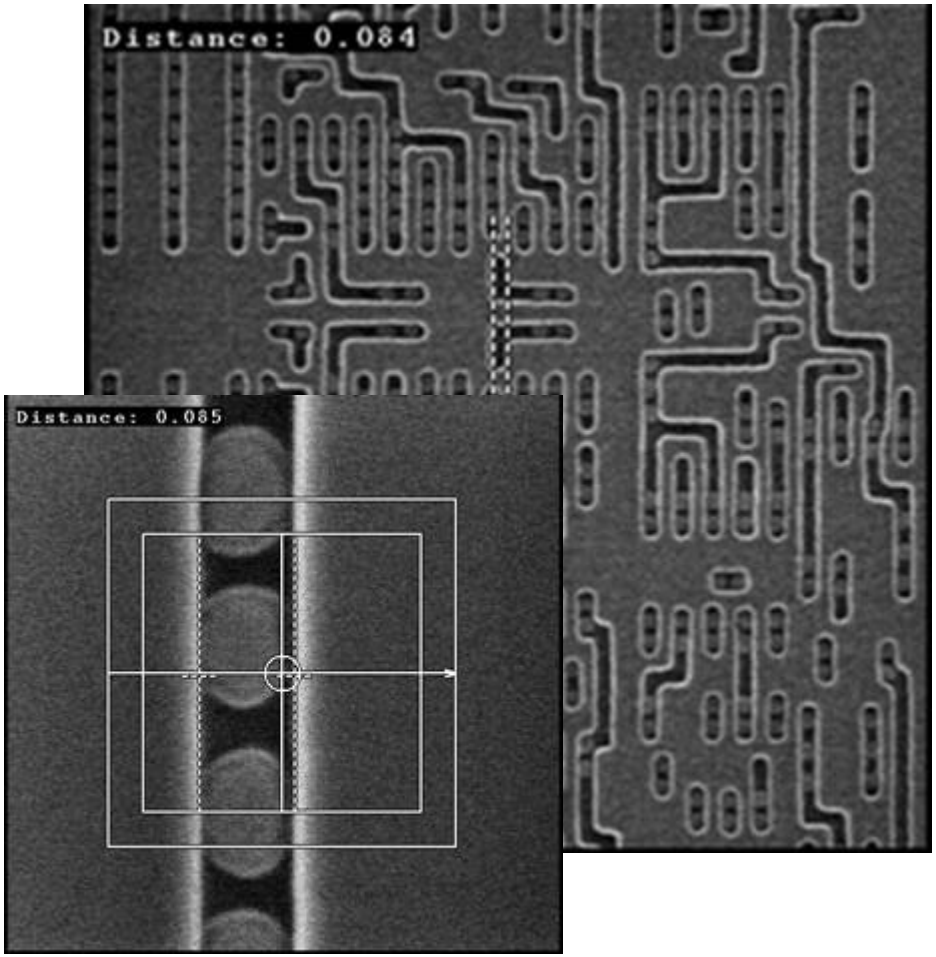
EUV Device Integration Roadmap

- EUVL feasibility is being demonstrated via a series of increasingly demanding device integration exercises
- This provides the truest test of the readiness of the technology and highlights the remaining critical issues

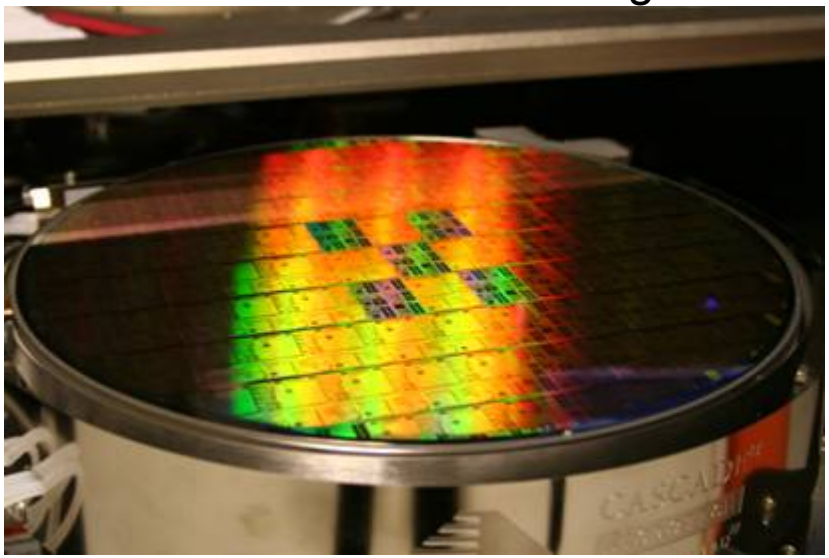


45-nm Node ‘Typhoon’ Product Demonstration

SEM Image showing alignment of etched trench over contacts



Photograph of 5 Chips Patterned at First Interconnect Level using EUVL

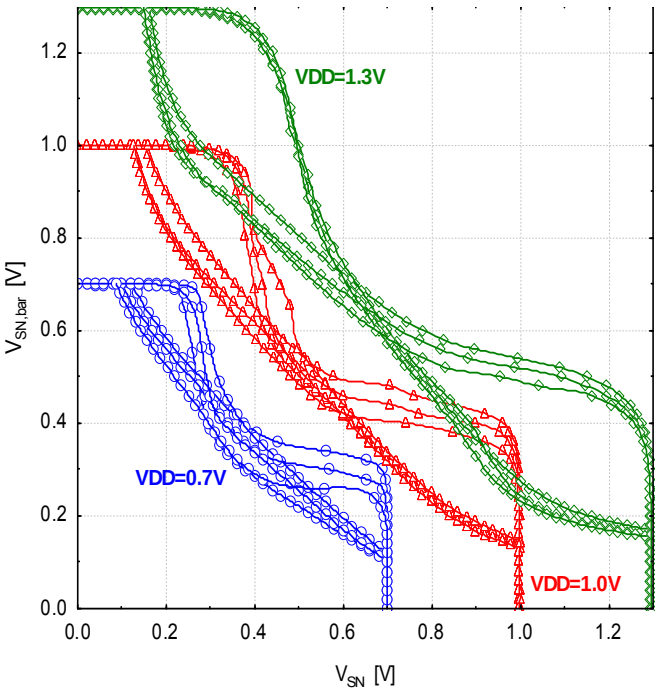


B. La Fontaine, et al., “The use of EUV lithography to produce demonstration devices,” Proc. SPIE 6921, 69210P (2008)

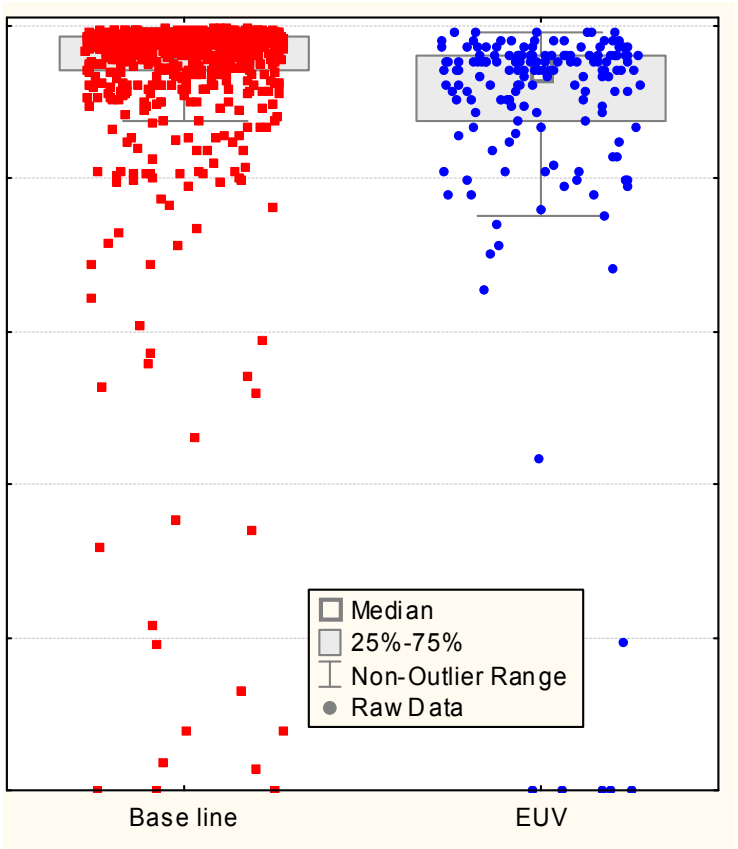
45-nm Node SRAM Functionality and Yield

- Only ~5% of defects on Typhoon mask blank appeared to print
- Only a few of those defects were found to be electrically critical

SRAM Butterfly Curves

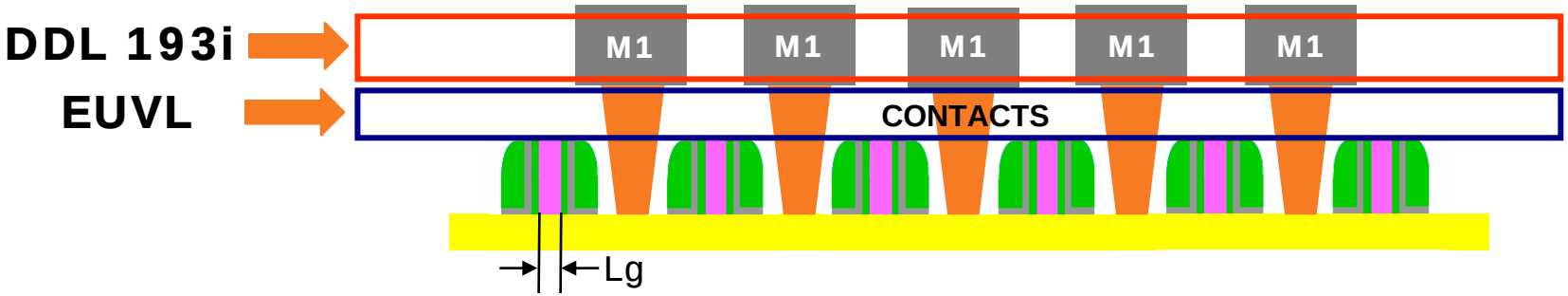


Normalized SRAM Yield

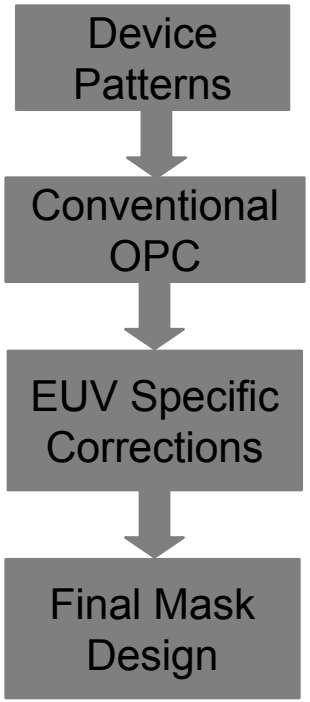


B. La Fontaine, "EUV lithography: Ready for manufacturing?" SEMICON West, July 15, 2009

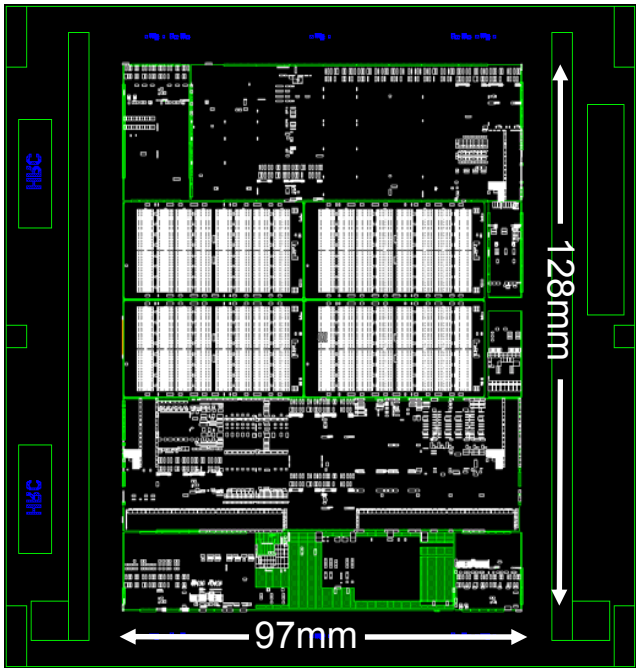
22-nm Node EUV Device Demonstration



Mask Pattern Correction



EUV Contact Level Mask

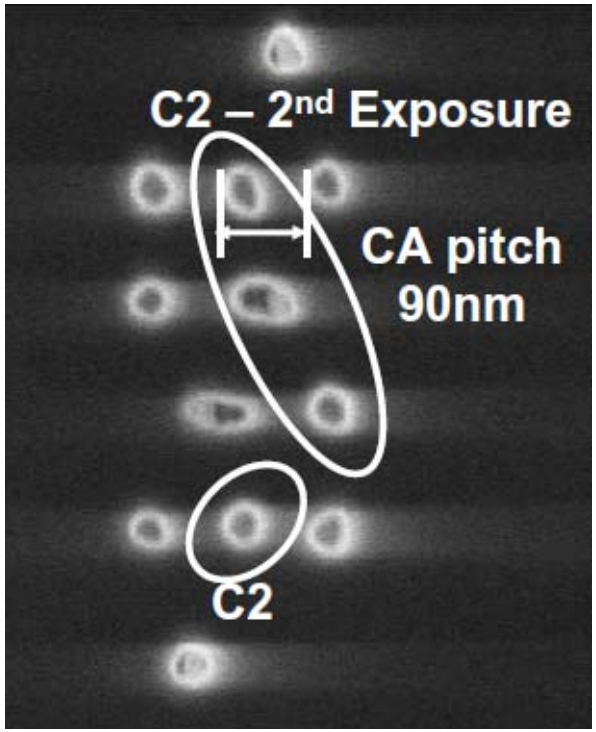


O. Wood, et al., "EUV lithography at the 22 nm technology node," Proc. SPIE 7636, 76361M (2010)

22-nm Node Contact Level Resist Images

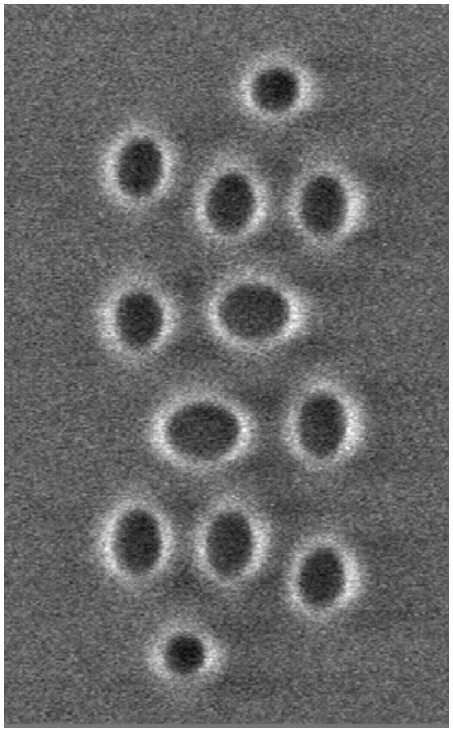
22-nm Node 6T SRAM Flycells

193i Pitch-Split DE²



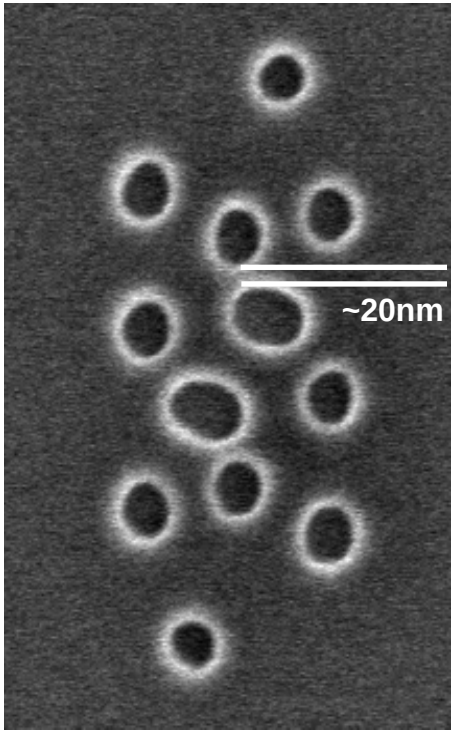
2008 IEDM
(0.100 μm²)

EUV SE Print



2009 SPIE
(0.080 μm²)

EUV SE Print



2009 EUVL Symp
(0.074 μm²)

- ~ 20 nm spaces between contacts are consistently resolved!

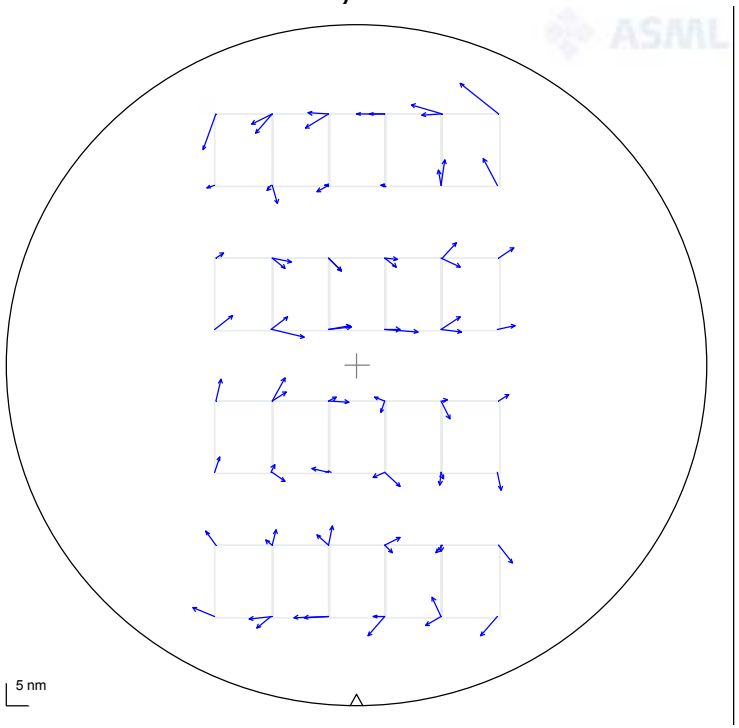
O. Wood, et al., "EUV lithography at the 22 nm technology node," Proc. SPIE 7636, 76361M (2010)

EUV to 193i Contact to Active Overlay

- Wafer stage temperature monitored until steady-state reached
- Maximum overlay errors were 9.2 nm in x and 11.2 nm in y

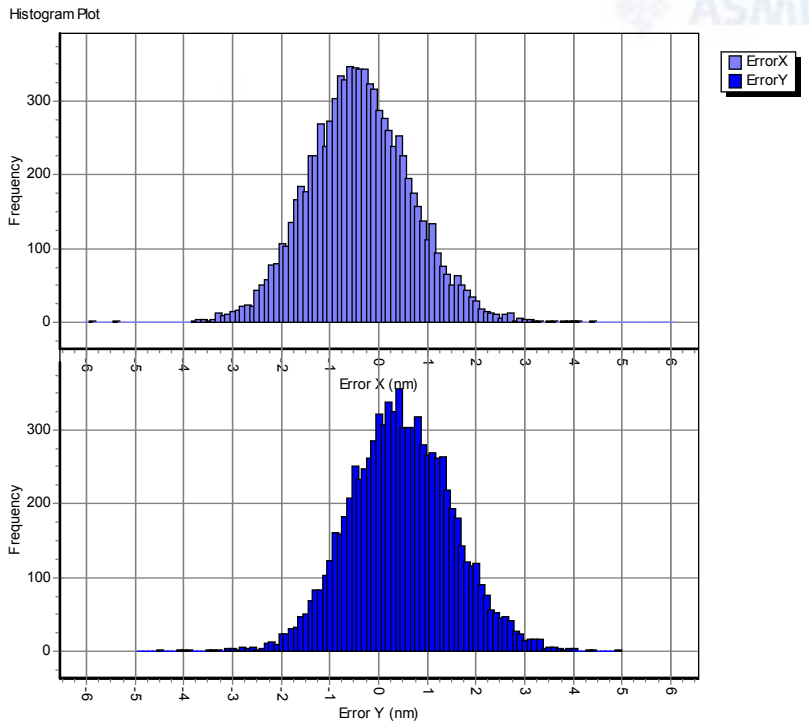
On-product Overlay Residuals

X = 8.0 nm, Y = 7.8 nm



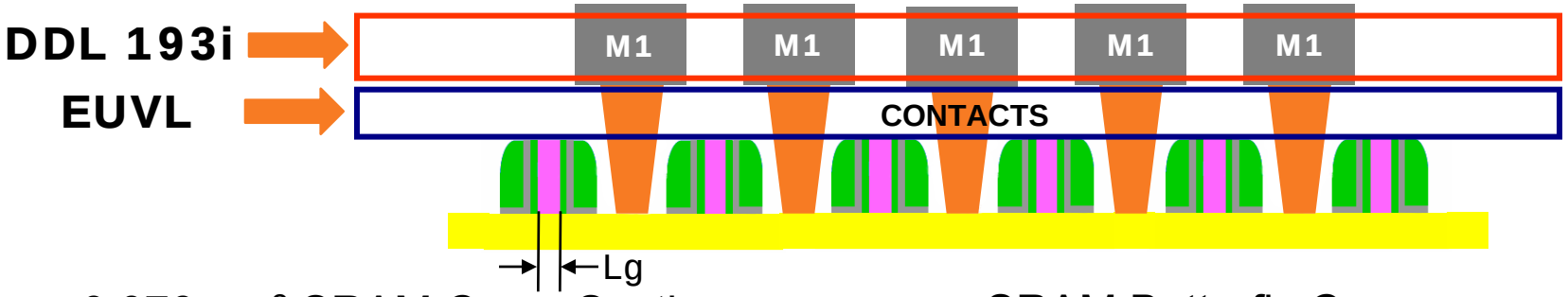
Single Machine Overlay

X = 2.2 nm, Y = 2.8 nm

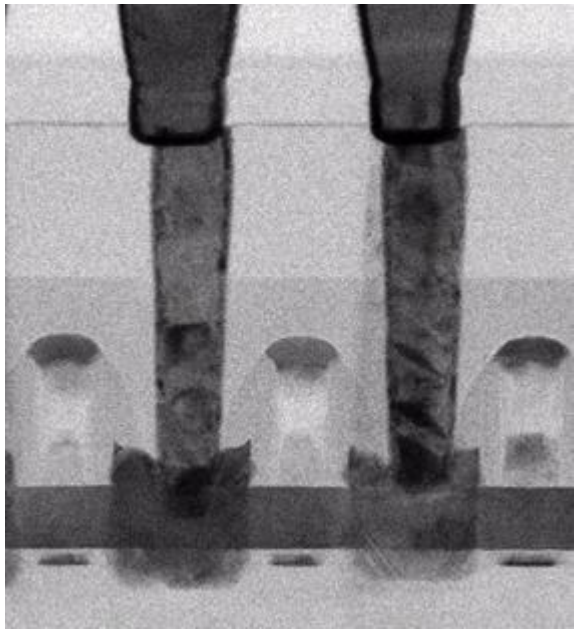


O. Wood, et al., "EUV lithography at the 22 nm technology node," Proc. SPIE 7636, 76361M (2010)

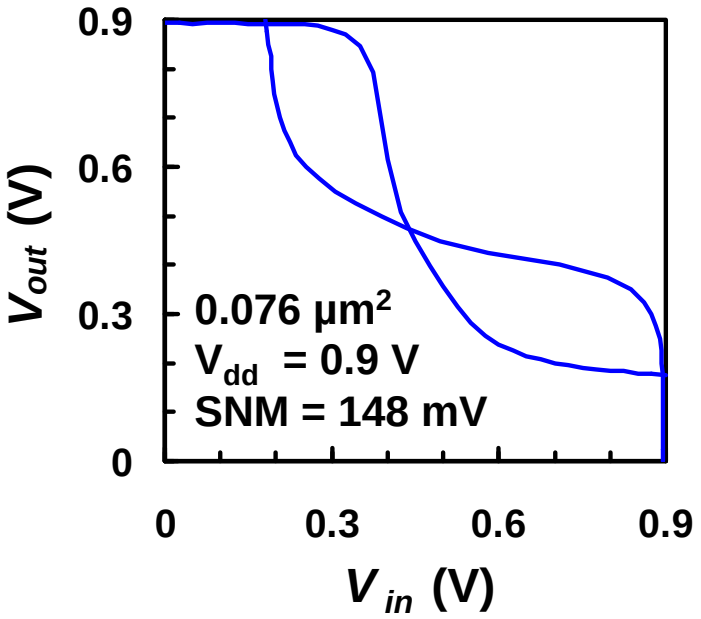
22-nm Node EUV Device Demonstration Result



0.076 μm² SRAM Cross Section



SRAM Butterfly Curve

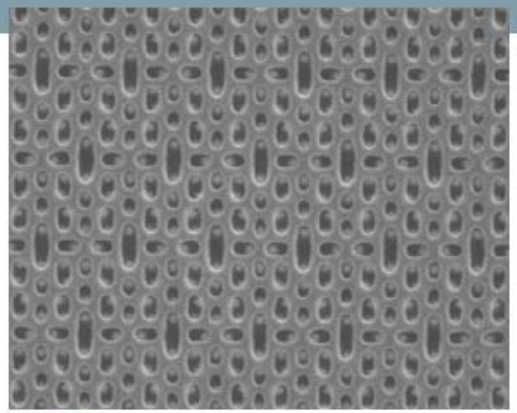


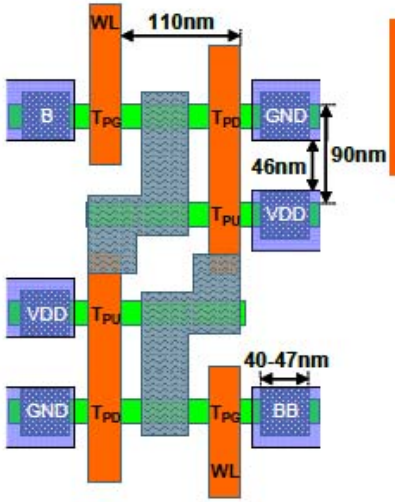
- Test chips with EUV CA level yielded nearly 100% of 0.076 μm² flycells

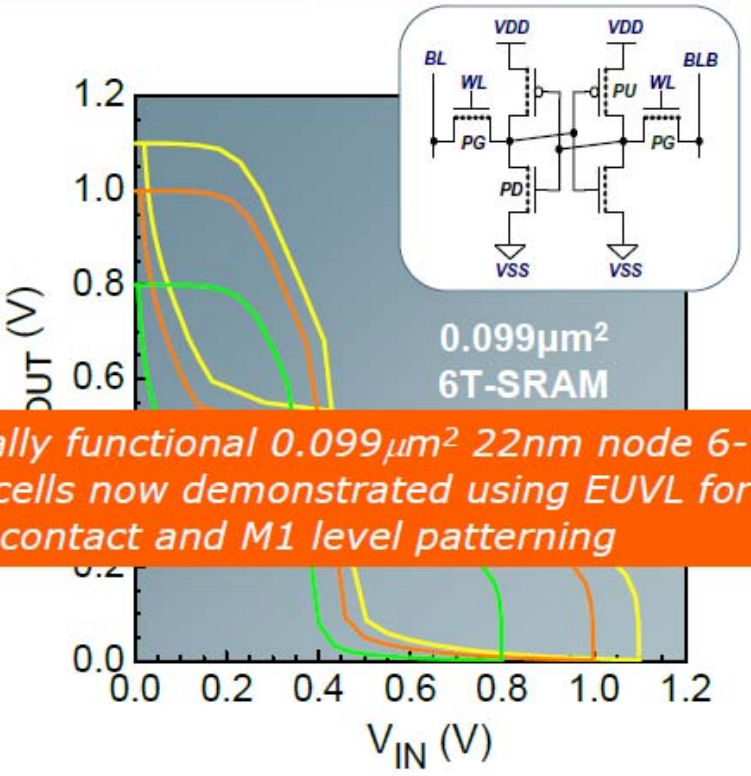
O. Wood, et al., "EUV lithography at the 22 nm technology node," Proc. SPIE 7636, 76361M (2010)

22-nm Node EUV Device Demonstration Result

Electrical data : butterfly curves





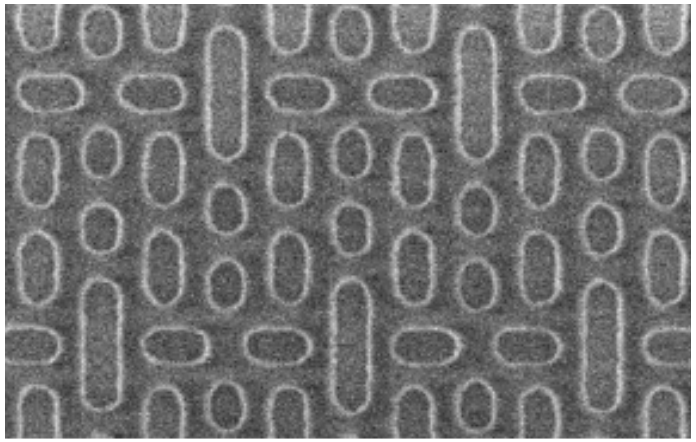


Electrically functional 0.099μm^2 22nm node 6-T SRAM cells now demonstrated using EUVL for contact and M1 level patterning

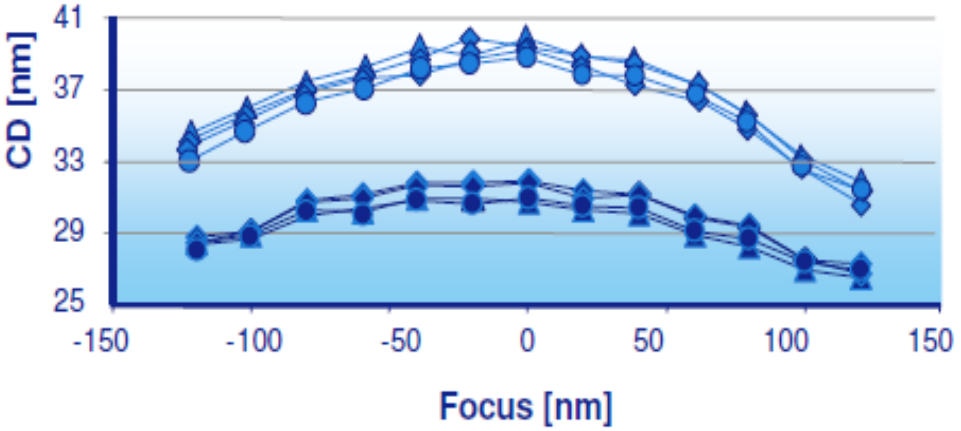
16-nm Node Contact Level Resist Image

- Single exposure EUV image of 0.042 μm^2 SRAM clip using 0.25 NA ADT

SEM data for a 16 nm SRAM clip



CD through focus for both C/H axes

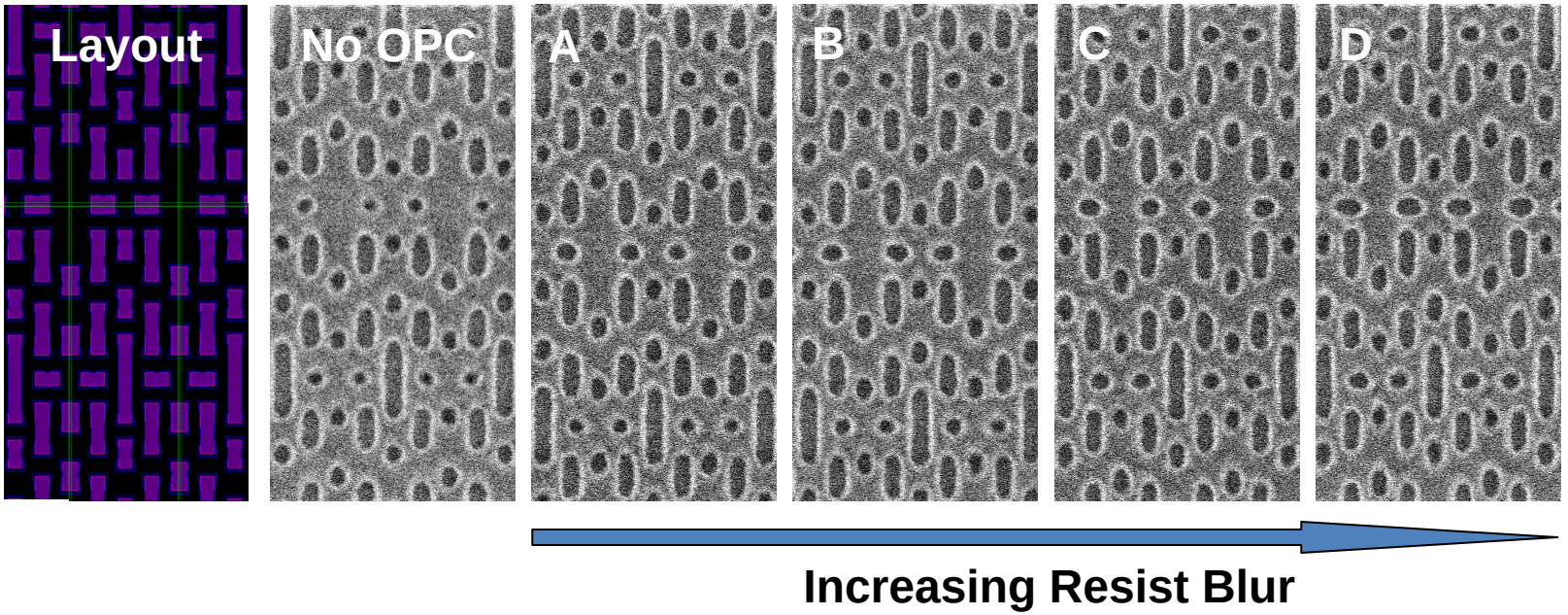


- X/Y-half pitch was 31/38 nm, leading to a cell size of 0.042 μm^2.
- Dose was 14 mJ/cm^2, exposure latitude was > 27%, and depth of focus was > 200 nm.
- Exposures were done without OPC, reticle error, or process corrections

C. Wagner, et al., "EUV into production with ASML's NXE platform," Proc. SPIE 7636, 76361H (2010)

16-nm Node Metal Interconnect Resist Image

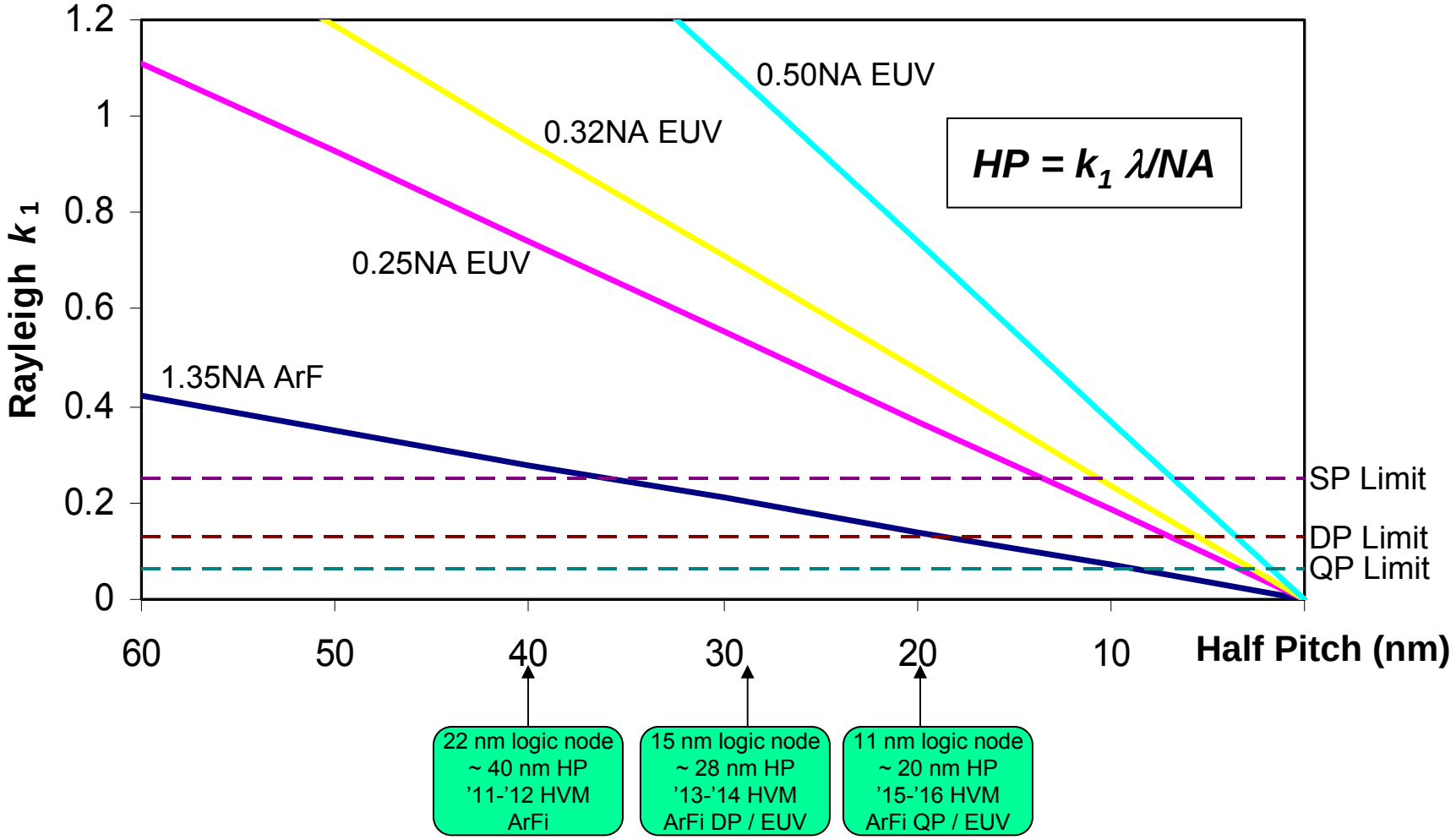
56 nm pitch M1 SRAM clips, SEVR-139, 75 nm thickness



- Patterns were corrected for EUV mask shadow effect before Mentor Graphics Calibre mnOPC resist models were applied
- No useful printability at 56 nm pitch without OPC
- All of the OPC models result in greatly improved process window overlap

O. Wood, et al., "EUV lithography at the 22 nm technology node," Proc. SPIE 7636, 76361M (2010)

Timing for High Volume Manufacturing Insertion



- Resolution below 10 nm is possible with high-NA EUV imaging optics

Full-Field EUV Exposure Tool Status

	ASML ADT	Nikon EUV1	ASML NXE:3100
			
Original Specs	NA = 0.25, σ = 0.5 Res = 40 nm 1:1 L/S Flare = 16% Overlay = 12 -15 nm TPT 6 – 10 WPH	NA = 0.25, σ = 0.8 (adj) Flare = 10% Overlay = 10 nm TPT 5 – 10 WPH	NA = 0.25, σ = 0.8 Res = 27 nm 1:1 L/S Flare = 8% Overlay = 4.5 nm TPT 60 WPH
Measured	Res = 26 nm 1:1 L/S POB WFE = 1.2 nm Flare = 12-14% Overlay = < 8 nm TPT 4 WPH (5 mJ resist)	Res = 26 nm (static mode) Res = 28 nm (scanning) POB WFE = 0.4 nm Flare = 7.5-9.5%	POB WFE = 0.8 nm Flare = < 7 % TPT < 60 WPH

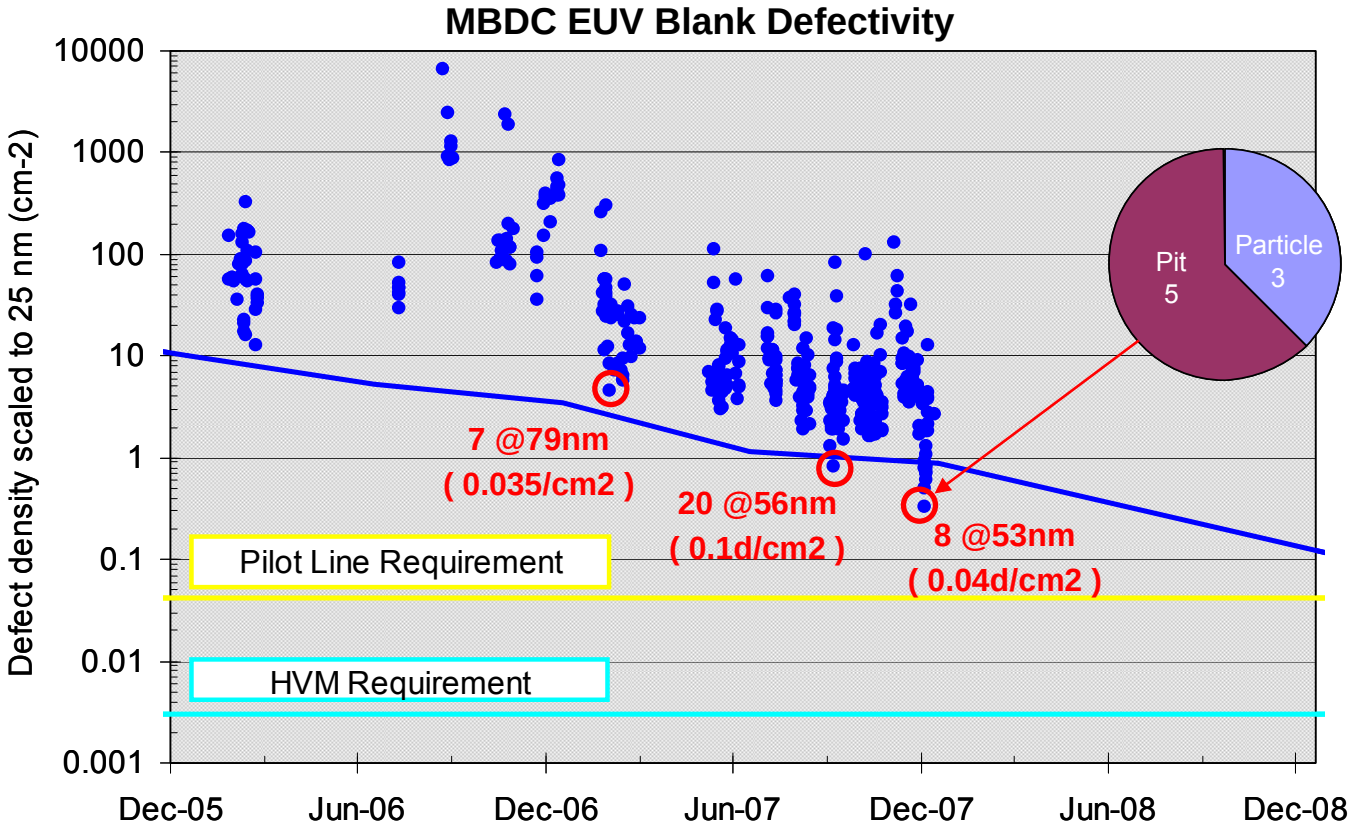
EUVL Infrastructure Status

Element	Metric	Current Status	15-nm Pilot Line Requirements (2011)
Mask	Blank Defectivity	0.04 defects/cm^2 @ 53 nm (champion) 0.09 defects/cm^2 @ 60 nm (~30% yield)	0.003 defects/cm^2 @ 25nm
	Reticle Handling	~0.1 adder per cycle @ 45 nm (~1 adder per cycle @ 25 nm PSL)	1 adder @ 25 nm
Source	Power at IF	14 W (DPP Source) 25 W (LPP Source)	100 W
	[1]Lifetime	100 Gpulses (1 year)	100 Gpulses (1 year)
Resist	Resolution	1:1 lines - 26 nm with DOF > 250 nm	28 nm with DOF > 150 nm
		Contacts - 28 nm with DOF > 150 nm	30 nm with DOF > 150 nm
	Sensitivity	12 mJ/cm^2 @ 26 nm L/S	< 20 mJ/cm^2
	[2]LER	2.5 nm (3σ) @ 32 nm & 15 mJ/cm^2	1.1 nm (3σ)
Optics	Quality	WFE ~ 0.4 nm rms MSFR ~ 0.07 nm rms	WFE < 0.7 nm rms MSFR < 0.1 nm rms
	Lifetime	>100 Gpulses	50 Gpulses

[1]Source head replacement / 10% reduction in collector reflectivity
[2]LER following post processing, i.e., using under layers, special rinse liquids, pattern transfer, etc.

EUV Mask Blank Defectivity Status

- Little progress in EUV mask blank defectivity since 2007
  - Champion plate in 2009 had 10 defects when inspected at 73 nm PSL sensitivity, 0.05 defects/cm^2

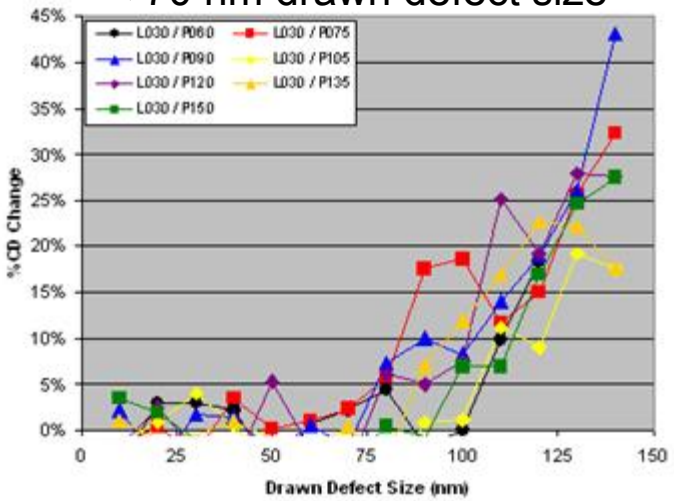


P. Kearney, et al., "Ion beam deposition for defect-free EUVL mask blanks," Proc. SPIE 6921, 69211X (2008)

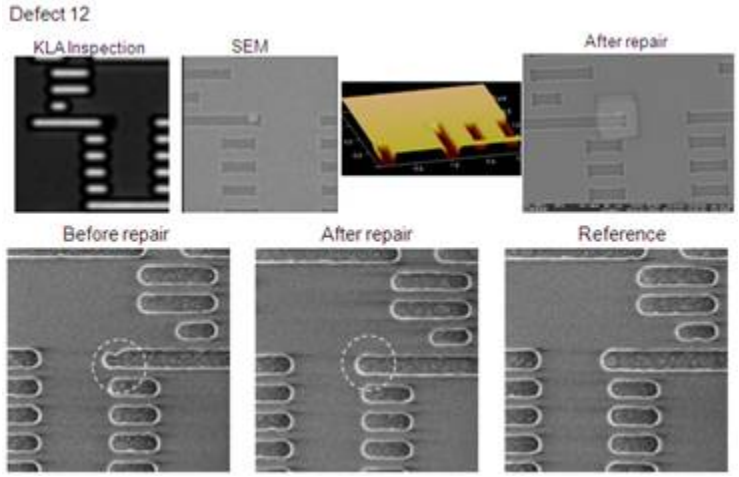
EUV Mask Defect Mitigation

- Last year Intel's EUV mask group succeeded in fabricating a zero defect reticle by:

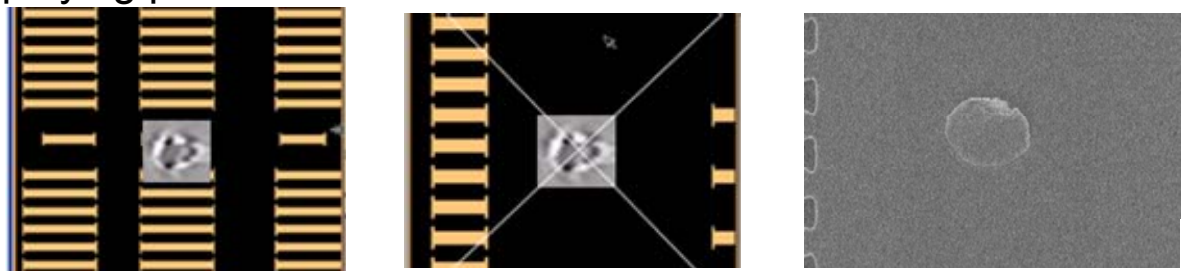
Restricting blanks to those with < 70 nm drawn defect size



Repairing absorber defects



Employing pattern shift so that defects were hidden in inactive areas



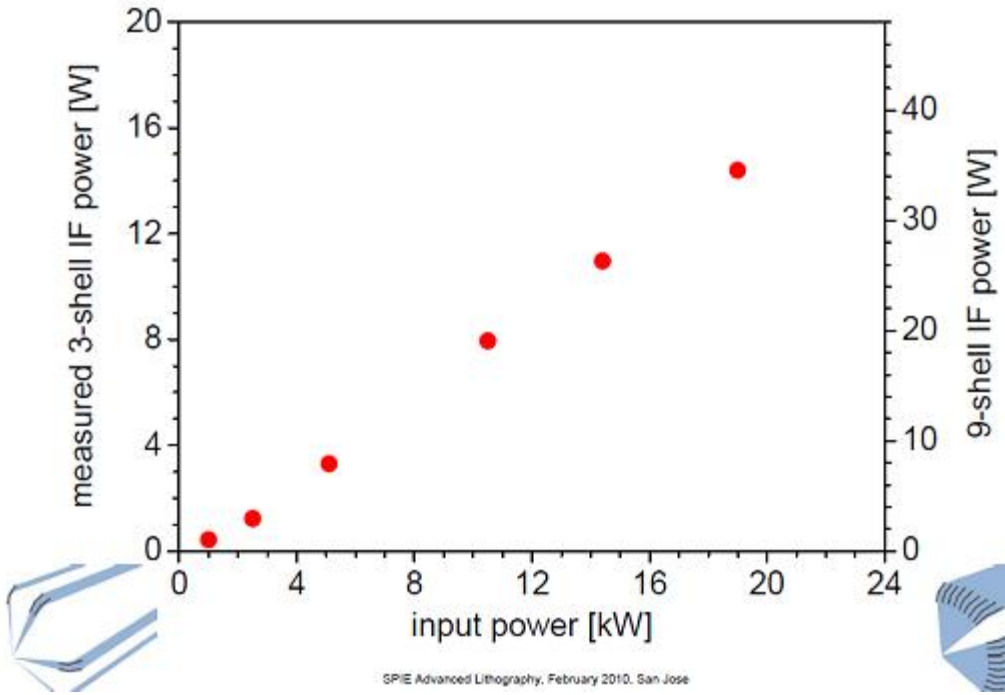
G. Vandentop, BACUS Technical Group Panel Discussion, SPIE Advanced Lithography 2010

EUV Discharge Produced Plasma Source Status

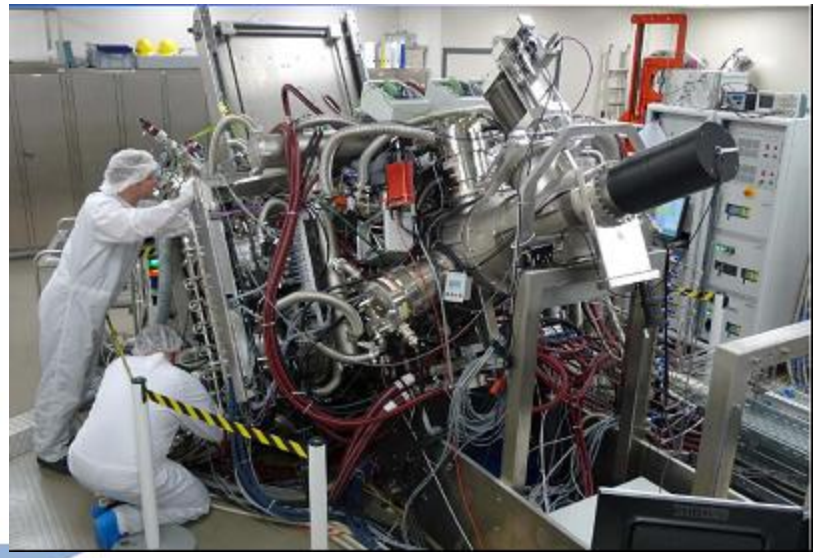
PHILIPS

XTREME technologies

- 14 W @ IF (100% DC) directly measured at IF with 3 shell collector optic
- 34 W @ IF with 9 shell collector scheduled to arrive in a few weeks
- Further power upgrade to 65 W and 105 W by frequency scaling of a few modules



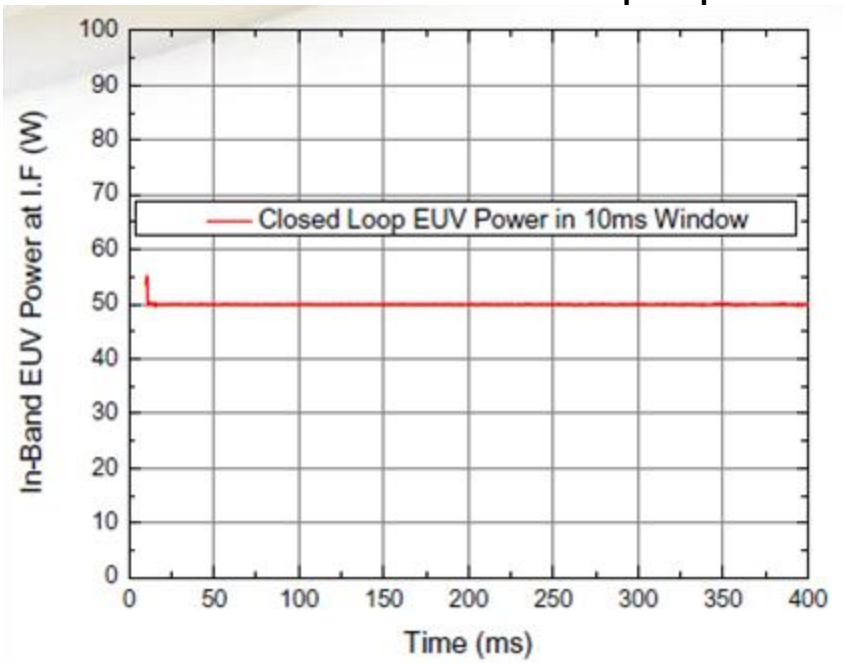
Sn DPP SoCoMo for NXE:3100



M. Corthout, et al., "Sn DPP SoCoMo integration for pilot phase and HVM," SPIE Advanced Lithography, Feb 2010, San Jose

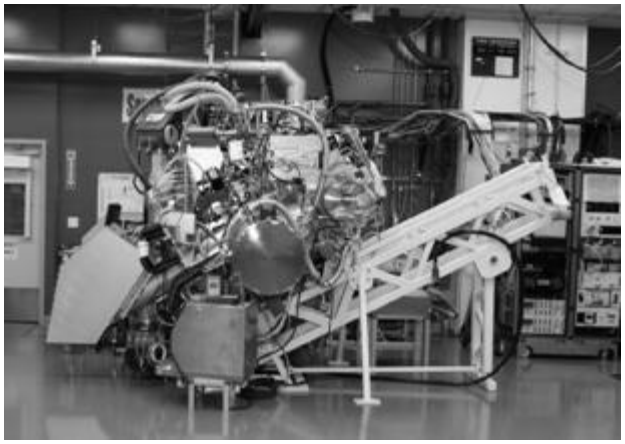
EUV Laser Produced Plasma Source Status

EUV LPP Source – Closed Loop Operation

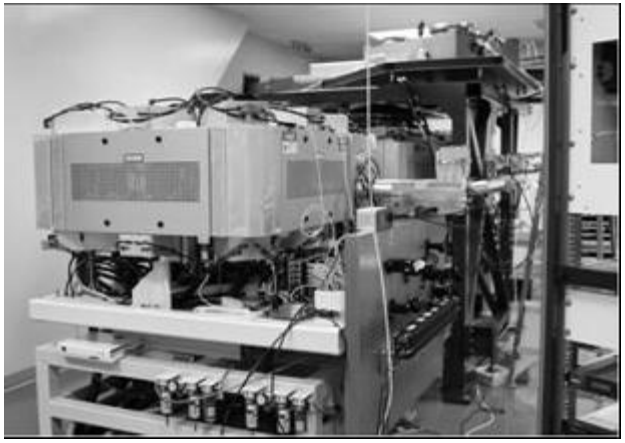


- 400 msec burst duration
- 80% duty cycle
- 30 μm diameter Sn droplets
- Power is measured at plasma and calculated at IF assuming 5 sr collection, 50% average reflectivity, and 90% transmission

Cymer HVM1 LPP Source Vessel



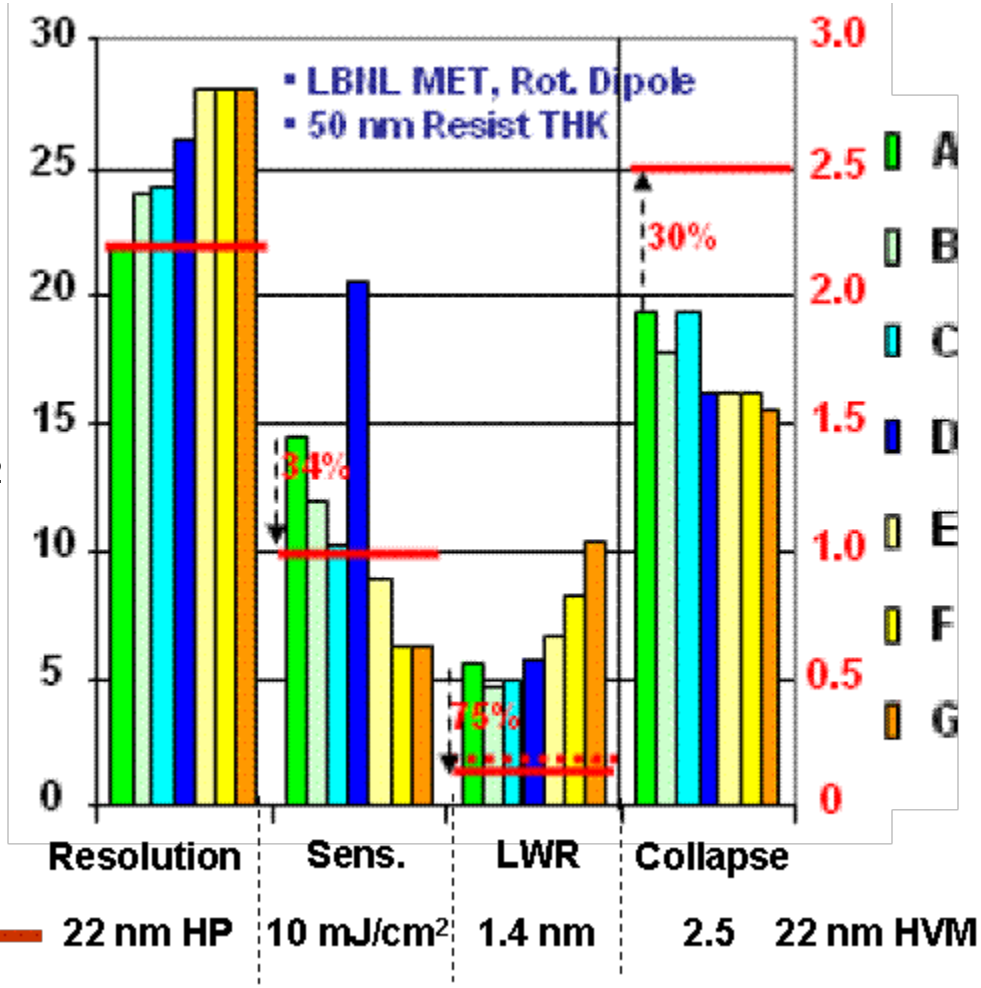
Cymer HVM1 CO_2 Drive Laser

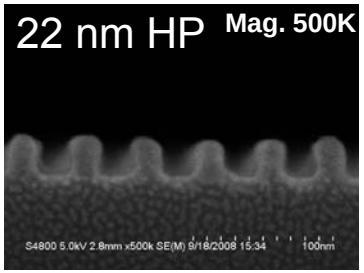


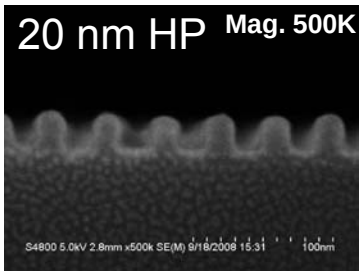
D. Brandt, et al., "LPP source system development for HVM," SPIE Advanced Lithography, Feb 2010, San Jose

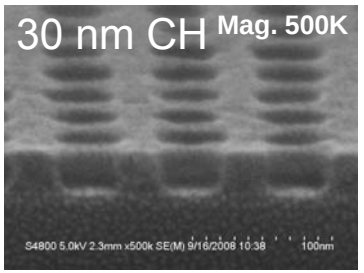
EUV Chemically Amplified Resist Status

- Resolution:
  - L/S ~ 20 nm
  - C/H ~ 30 nm
- Sensitivity:
  - L/S ~ 15 mJ/cm^2
  - C/H ~ 50 mJ/cm^2
- Line Edge Roughness:
  - L/S ~ 4 - 5 nm
  - C/H ~ TBD



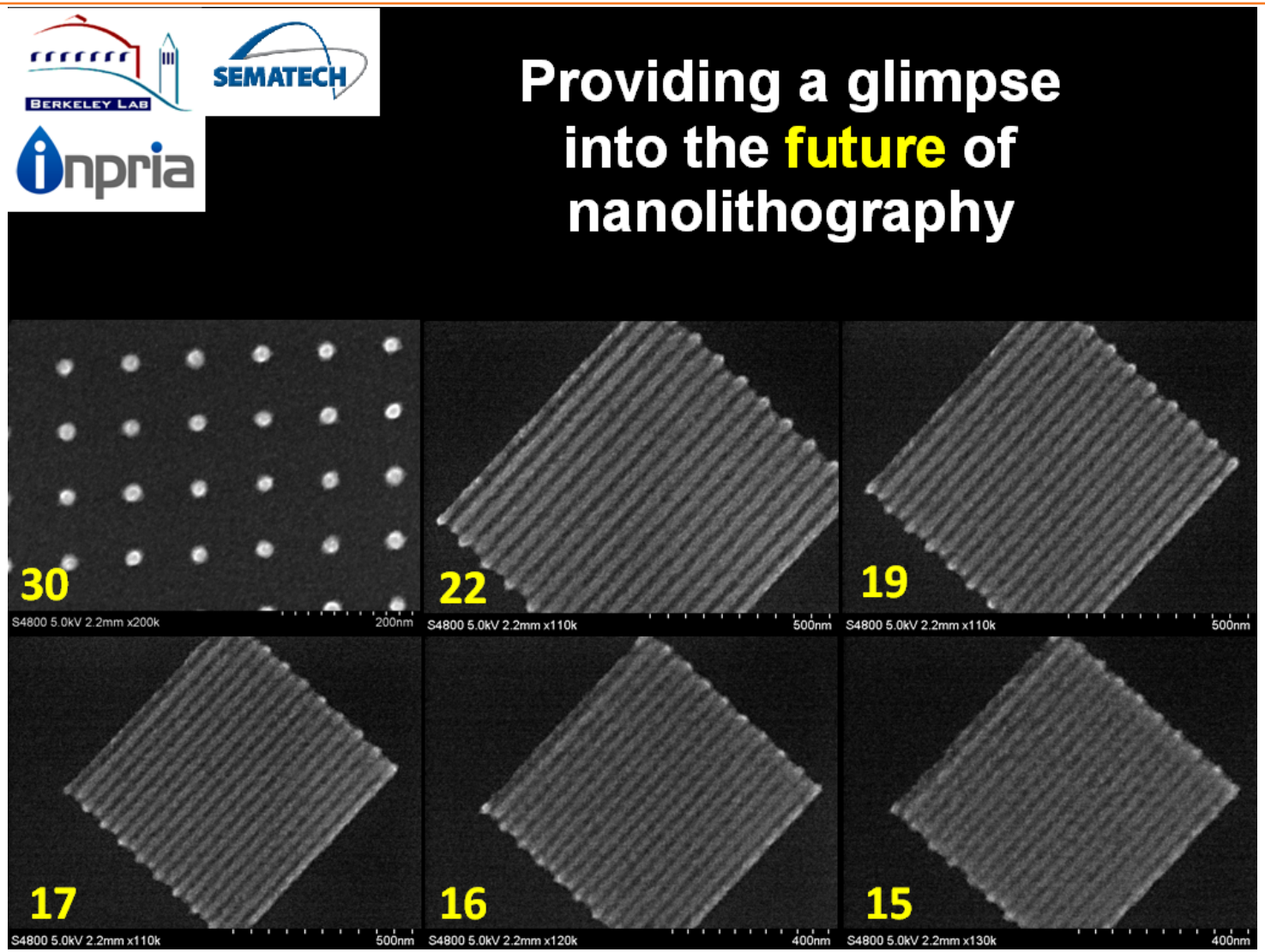






C. Koh, et al., "Characterization of promising resist platforms for sub-30 nm HP manufacturability and EUV CAR extendibility study," Proc. SPIE 7636, 763604 (2010).

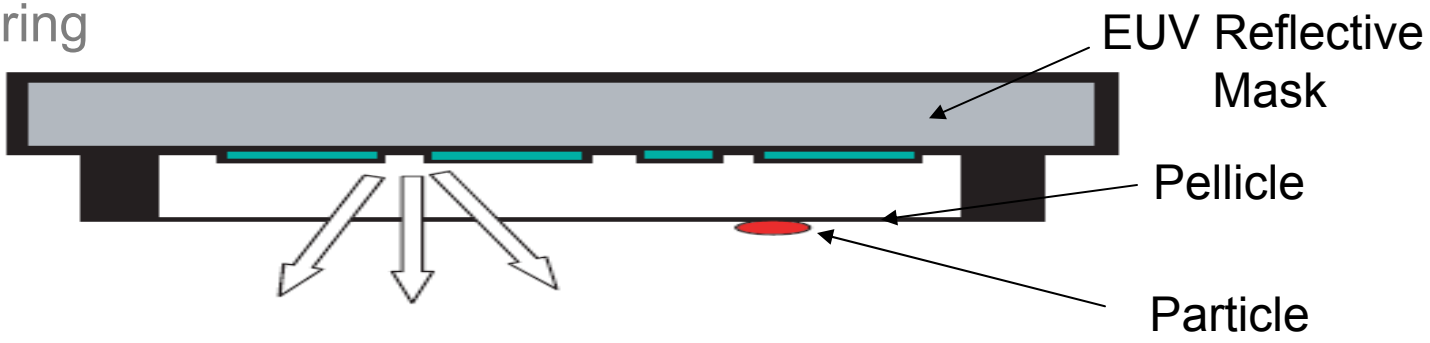
EUV Non-Chemically-Amplified Resist



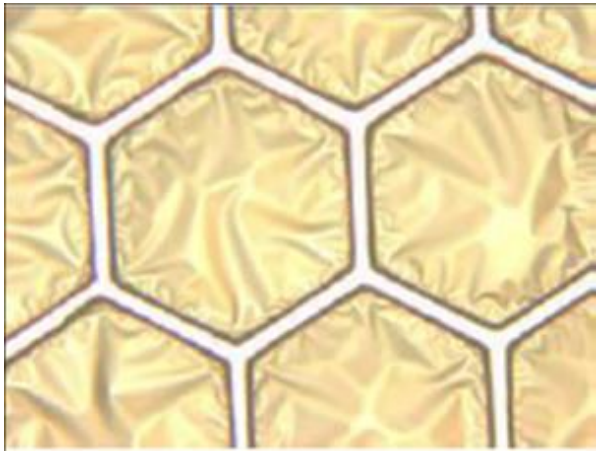
P. Naulleau, "The SEMATECH Berkeley MET pushing EUV development beyond 22-nm half pitch," Proc. SPIE 7636, 76361J (2010)

EUV Mask Pellicle

- A viable non-removable mask pellicle may be needed for high-volume manufacturing

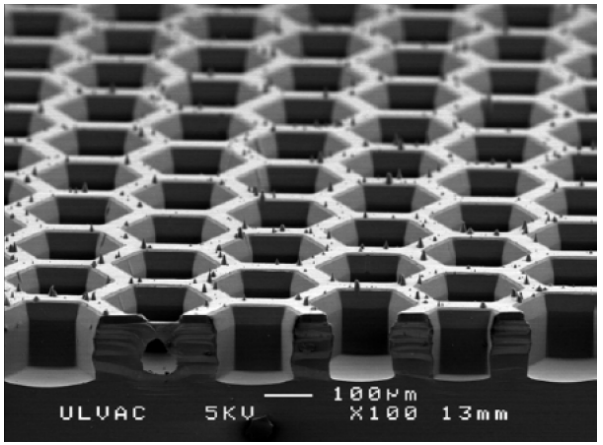


75 nm Si membrane on wire mesh



Y. Shroff, et al., "EUV pellicle development for mask defect control," Proc. SPIE 6151, 615104 (2006).

100 nm Si membrane on honeycomb

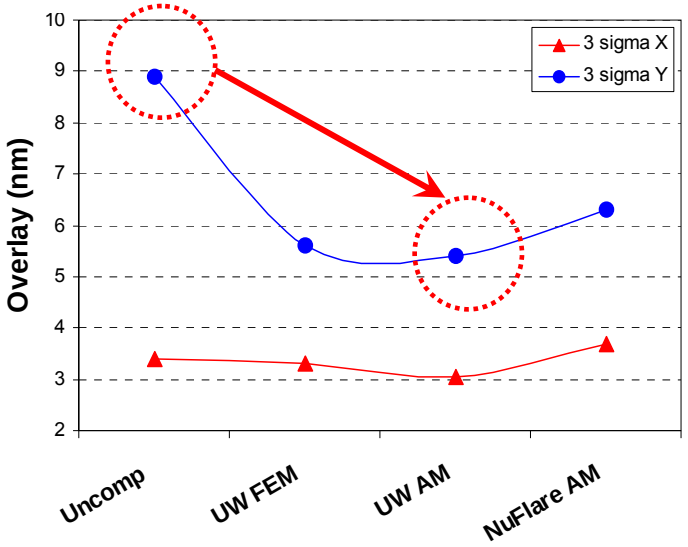


S. Akiyama & Y. Kubota, "Realization of EUV pellicle with single crystal silicon membrane," 2009 EUVL Symposium, Prague

EUV Mask Flatness Compensation

- EUV mask flatness needs to be ~30nm to meet overlay specs, but aggressive polishing adds defects and increases cost
- Goal: use flatness compensation to relax spec 10x to 300nm
- Masks with ~ 400 nm bow tested on ADT for overlay performance

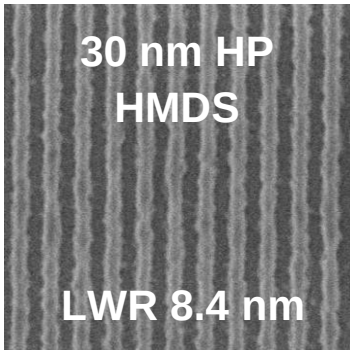
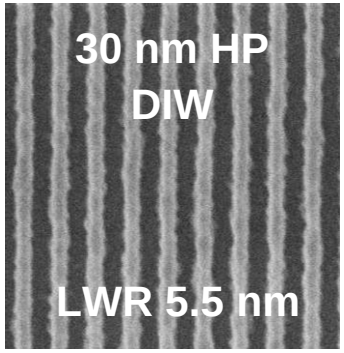
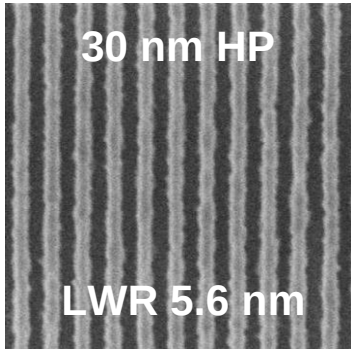
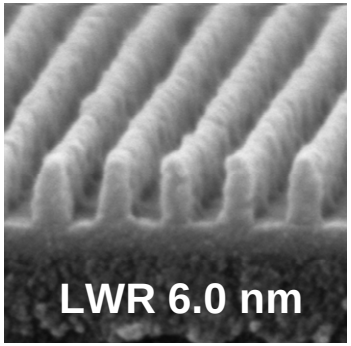
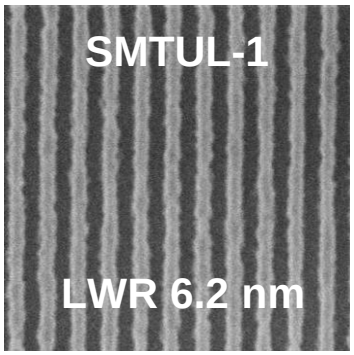
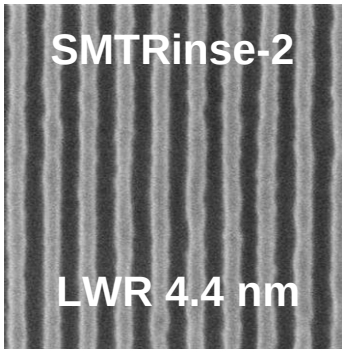
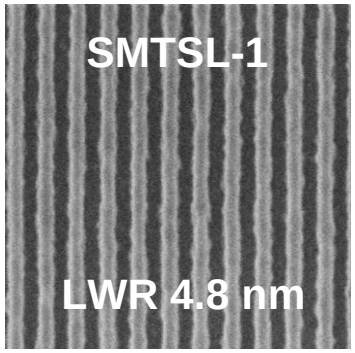
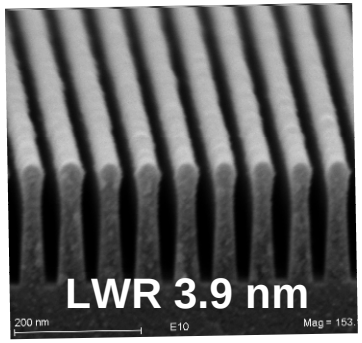
Layout	x_{max}	$3\sigma_x$	y_{max}	$3\sigma_y$
Uncomp	3.5	3.4	6.8	8.9
UW FEM	3.2	3.3	4.3	5.6
UW AM	3.1	3.1	4.9	5.4
NuFlare AM	3.2	3.7	5.0	6.3



- Flatness compensation shown to produce 39% improvement

S. Raghunathan, "A study of image placement error from reticle non-flatness in extreme ultraviolet lithography," PhD Thesis Defense, College of Nanoscale Science and Engineering, April 27, 2010

LWR Improvement at Each Process Step

30 nm HP	Underlayer	Rinse Material	Smoothing Layer Attachment	Pattern Transfer
Baseline				
LWR improvement process				
LWR improvement	2.2 nm (27%)	1.1 nm (20%)	0.8 nm (14%)	2.1 nm (35%)

C. Koh, et al., "Characterization of promising resist platforms for sub-30 nm HP manufacturability and EUV CAR extendibility study," Proc. SPIE 7636, 763604 (2010).

Summary

- Advantages of EUV lithography are wide process windows, high throughput (once source power specs are met), and extendibility.
- Disadvantages of EUV lithography are higher costs & complexity (than single exposure ArFi lithography) and infrastructure immaturity.
- EUV litho with the ADT at the 22 nm logic node is considerably easier & results in higher device yield than double-exposure double-etch ArFi litho.
- HVM EUV exposure tools will be available starting in 2012.
- Mask blank defectivity and source power at IF are not yet at the levels needed for 15-nm node pilot production.
  - Defect repair, defect avoidance, and defect compensation techniques will be needed for finite mask yield.
  - Current 193-nm based defect inspection tools offer an interim solution for EUV mask inspection.
- Reticle handling, optics quality and lifetime, and resist resolution and sensitivity are close to spec; resist LER is not. LER reduction via post processing will be required.
- Topics that need additional development include: mask defect mitigation, mask pellicles, mask flatness compensation, and LWR reduction.

Acknowledgements

- ASML: Kevin Cummings, Noreen Harned, & Christian Wagner
- CNSE: Sudhar Raghunathan
- Cymer: David Brandt and Nigel Farrar
- GLOBALFOUNDRIES: Yunfei Deng, Bruno La Fontaine, Harry Levinson, Uzodinma Okoroanyanwu, & Tom Wallow
- IBM: Matthew Colburn, Gregory McIntyre, & David Medeiros
- IMEC: Mieke Goethals
- Intel: Janice Golda, Ted Liang, Yashesh Shroff, & Gilroy Vandentop
- LBNL: Patrick Naulleau
- Philips Extreme UV/XTREME: Marc Corthout & Masaki Yoshioka
- SEMATECH: David Chan, Patrick Kearney, Chawon Koh, & Stefan Wurm
- Shin-Etsu: S. Akiyama & Y. Kubota
- Toshiba America Electronic Components: Hiroyuki Mizuno